Intel® Itanium™ Processor

Specification Update

December 2001

Notice: The Intel® Itanium™ processor may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

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Contents

Revision History

Version Number	Description	Date
001	This document is the first specification update for the Intel® Itanium™ processor.	June 2001
002	Updated status for erratum 4 and erratum 10. Updated workaround for erratum 14. Added errata 22-24.	July 2001
003	Updated workaround for erratum 24. Added PAL version 6.6.24 to the Errata Summary Table. Added errata 25-27.	August 2001
004	Updated workaround for erratum 9. Added PAL version 6.6.25 to the Errata Summary Table. Added erratum 28.	September 2001
005	Updated workaround for errata 14 and 24. Updated fix status for erratum 24. Added PAL version 6.6.26 to the Errata Summary Table. Added errata 29-31.	December 2001

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents in the table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Affected Documents/Related Documents

Title	Document #
Intel® Itanium™ Processor at 800 MHz and 733 MHz Datasheet, Rev 1.0	249634
Intel® Itanium™ Processor Hardware Developer's Manual, Rev 1.0	248701
Intel® Itanium™ Architecture Software Developer's Manual, Volume 1: IA-64 Application Architecture	245317
Intel® Itanium™ Architecture Software Developer's Manual, Volume 2: IA-64 System Architecture	245318
Intel® Itanium™ Architecture Software Developer's Manual, Volume 3: Instruction Set Reference	245319
Intel® Itanium™ Architecture Software Developer's Manual, Volume 4: Itanium™ Processor Programmer's Guide	245320
Intel® Itanium™ Architecture Software Developer's Manual Specification Update	248699
Intel® Itanium™ Processor Family System Abstraction Layer Specification (available on the web)	245359

Nomenclature

S-Spec Number is used to identify products. Products are differentiated by their unique characteristics, e.g. core speed, L3 cache size, package types, etc. Care should be taken to read all notes associated with each S-Spec number.

Errata are design defects or errors. Errata may cause the Intel® Itanium™ processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given processor must assume that all errata documented for that stepping are present on all devices unless otherwise noted.

Specification Changes are modifications to the current published specifications for the Itanium processor. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

General Information

Intel® Itanium™ Processor Cartridge Marking

The cartridge mark for the product is a laser marked label attached to the end of the PAC418 cartridge opposite the power tab. The mark provides the following information:

- Product brand name
- Manufacture traceability (including manufacturing lot and unit identification)
- Manufacturing site
- Mask work and copyright protection for the processor and cache die
- Product identification (including processor core speed, cache size, bus speed)
- Intel company logo
- Two-dimensional product identification matrix for Intel internal use

FFFFFFFF - manufacture traceability number
NNNN - serial number
yy - year

Intel® Itanium™ Processor Identification and Package Information

S-Spec/QDF Number	Core Stepping	CPUID	Speed (MHz)	L3 Size (Mbytes)	Notes
SL4LT	C0	0007000604h	733/133	2	a
SL4LS	C0	0007000604h	733/133	4	a
SL4LR	C0	0007000604h	800/133	2	a
SL4LQ	C0	0007000604h	800/133	4	a

a. The CPUID column in this table indicates the contents of bits 39:0 of CPUID Register 3. Bits 63:40 of this register are reserved

Mixed Steppings in MP Systems

The Itanium processor supports multi-processor platforms using mixed processor steppings of N and N-1 on the same system bus. While Intel has done nothing to specifically prevent processors within a multi-processor environment from operating with mixed steppings beyond the N and N-1 configurations, there may be uncharacterized errata that exist in such configurations.

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Itanium processor steppings. Intel may fix some of the errata in a future stepping of the component or in a future release of the Processor Abstraction Layer (PAL), and account for the other outstanding issues through documentation or specification changes as noted. This table uses the notations indicated below.

Codes Used in Summary Table of Changes

Stepping

X:	Errata exists in the stepping or PAL version indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping or PAL version.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component, or in a future release of PAL.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of this document.

Errata Summary Table

Errata

No.	Processor Stepping	PAL Version					Pg	Status	Errata
	C0	6.6.21	6.6.23	6.6.24	6.6.25	6.6.26			
1	X						12	NoFix	IFA may contain incorrect address
2	X						12	NoFix	AR.ITC returns an incorrect value
3	X						12	NoFix	L1D line fill during DBR/IBR access may result in an incorrect line fill
4	X						12	NoFix	IA-32: Incorrect self-modifying code behavior
5	X						13	NoFix	System bus pins driven low during JTAG continuity testing
6	X						13	Fix	INIT# signal not recognized properly
7		X					13	Fixed	BINIT condition prevents error logging
8	X						13	NoFix	Internal BINIT during low power light halt mode
9	X						13	NoFix	Incorrect error logging information for double-bit ECC error on PTC or interrupt transaction
10	X						14	NoFix	Processor hang during nested BINIT
11		X	X				14	Fixed	False BIL transactions during PAL_CACHE_FLUSH
12	X						14	Fix	ALL_STOPS_DISPERSED and EXPL_STOPS_DISPERSED not operating correctly
13	X						14	NoFix	Snoop hit to modified line in L2 cache with tag parity error
14	X						15	Fix	Infinite DBSY# hang due to livelock condition
15	X						15	NoFix	Unexpected writeback transaction in 2:11 mode with bus parking enabled
16	X						15	Fix	IA-32: Code with FP instruction followed by integer instruction with interrupt pending may not execute correctly
17		X					16	Fixed	Bus parking always enabled and not controllable by PAL
18		X	X				16	Fixed	IA-32: FSINCOS may not generate FP precision exception
19	X						16	NoFix	chk.a.clr/ld.c.clr incorrectly clears its ALAT entry
20	X						16	Fix	IA-32: Back to back semaphores under certain circumstances may cause processor to hang
21	X						17	Fix	Modification of PFS under certain circumstances can lead to unexpected program behavior
22		X	X				17	Fixed	Corrected machine check not indicated when CMCI is promoted to MCA
23		X	X				17	Fixed	PAL_MC_ERROR_INFO may return incorrect target address information
24	X						17	NoFix	Incorrect store update to L1D cache under certain circumstances
25	X						18	NoFix	IA-32: Unexpected page fault exception on SETcc instruction
26	X						18	NoFix	IA-32: PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ reads 8 bytes instead of 4 bytes
27	X						18	NoFix	Processor may incorrectly report an IA-32 BIST failure
28	X						18	Fix	Back-to-back pair of loads to L1D cache result in possible livelock condition
29		X	X	X	X	X	19	Fix	PAL_PERF_MON_INFO returns incorrect information on registers which can count retired instruction bundles
30	X						19	NoFix	ALAT not guaranteed to be invalidated by an external snoop under specific conditions
31	X						19	NoFix	WC store may be dropped under certain conditions

Specification Changes

No.	Processor Stepping	PAL Version					Pg	Status	SPECIFICATION CHANGES
	C0	6.6.21	6.6.23	6.6.24	6.6.25	6.6.26			
									None for this revision of the Specification Update

Specification Clarifications

No.	Processor Stepping	PAL Version					Pg	Status	SPECIFICATION CLARIFICATIONS
	C0	6.6.21	6.6.23	6.6.24	6.6.25	6.6.26			
									None for this revision of the Specification Update

Documentation Changes

No.	Processor Stepping	PAL Version					Pg	Status	DOCUMENTATION CHANGES
	C0	6.6.21	6.6.23	6.6.24	6.6.25	6.6.26			
									None for this revision of the Specification Update

Errata

1. IFA may contain incorrect address

Problem: The Interruption Fault Address (IFA) is not correctly reported for Instruction Access faults and Instruction Debug faults when the processor is executing Itanium instructions. The IFA is reported correctly when the processor is executing IA-32 instructions.

Implication: The IFA may report a wrong IP address on an Instruction Access-bit access or an Instruction Debug fault. Operating systems should not rely on the value in IFA when these faults occur.

Workaround: The IIP (Interruption Instruction Bundle Pointer) provides the same information as the IFA for Instruction Access faults and Instruction Debug faults. These fault handlers should use the IFA or the IIP based on IPSR.is:

```
if (IPSR.is)
       use IFA
else
       use IIP
```

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

2. AR.ITC returns an incorrect value

Implication: The 64-bit Interval Timer Counter register (AR.ITC) may return an incorrect value when the lower 32-bits are all F's. In this case, the value returned in the upper 32-bits is incremented by 1. For example, when the value returned is 0x1FFFFFFFF, the actual value should be 0x0FFFFFFFF.

Implication: Software that utilizes the AR.ITC register will receive an incorrect value in this case.

Workaround: The workaround is for software to re-read the AR.ITC register when it detects all F's in the lower 32-bits.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

3. L1D line fill during DBR/IBR access may result in an incorrect line fill

Implication: Under certain circumstances, if a line fill to the L1 data cache occurs simultaneously with Debug Breakpoint Register (DBR/IBR) accesses, the line fill to the L1 data cache may incorrectly occur to address zero. In general, this erratum can be encountered if the code sequence contains a 'Move to Data Breakpoint Register' instruction followed by a 'Move to Instruction Breakpoint Register' instruction.

Implication: Code that operates on the debug breakpoint registers in the above sequence may possibly overwrite address zero data. Subsequent use of this data may result in unpredictable behavior.

Workaround: Insert a serializing instruction 'srlz.d' in between the 'mov dbr' and the 'mov ibr' instruction.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

4. IA-32: Incorrect self-modifying code behavior

Problem: Under certain circumstances, the processor may fail to correctly execute IA-32 self-modifying code (SMC). In the failing scenario, the processor does not wait for a previous store to complete prior to issuing and completing an instruction fetch to the same address.

Implication: IA-32 SMC may execute incorrectly resulting in unexpected program behavior.

Workaround: A workaround for this erratum is implemented in PAL 6.6.21 and later versions.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

5. System bus pins driven low during JTAG continuity testing

Problem: During JTAG Boundary Scan continuity testing, the system bus pins may be driven low by the processor not allowing the pins to be forced to a high state.

Implication: The system bus RESET# pin cannot be tested for continuity as board-level component interconnect testing requires the system bus RESET# pin to be kept asserted.

Workaround: Assert the system bus RESET# pin during JTAG Boundary Scan continuity testing.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

6. INIT# signal not recognized properly

Problem: The INIT# signal triggers an unmasked interrupt to the processor. When operating at the 2:11 bus-to-core frequency ratio, the assertion of the INIT# pin may not always be recognized by the processor, preventing the processor from taking the interrupt.

Implication: The processor may miss taking the INIT# interrupt when operating at the 2:11 bus-to-core frequency ratio. Note: This erratum does not impact the use of the INIT# pin for power-on configuration during reset.

Workaround: Either a system bus-based interrupt transaction or the Platform Management Interrupt (PMI)# input can be used to implement the same functionality.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

7. BINIT condition prevents error logging

Problem: On a BINIT non-recoverable Machine Check Abort (MCA) condition, the processor may enter an infinite loop in the PAL MCA handler. This prevents hand-off to the SAL MCA handler from occurring.

Implication: On a BINIT MCA condition, the processor may encounter a hang. This will prevent the BINIT error from being logged. Note: Since BINIT indicates that a fatal condition has occurred which prevents reliable future operation, the system would normally be reset.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

8. Internal BINIT during low power light halt mode

Problem: The processor enters a light halt mode upon executing either the PAL_HALT_LIGHT or the PAL_HALT_LIGHT_SPECIAL calls. During light halt mode, if the processor encounters an internal BINIT (Bus Initialization) non-recoverable MCA condition, the processor may not flag the MCA as expected.

Implication: The processor may not flag the fatal error condition as expected during light halt mode.

Workaround: Flush and invalidate all cache lines by calling the PAL_CACHE_FLUSH call with inv = 1 before entering the light halt mode.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

9. Incorrect error logging information for double-bit ECC error on PTC or interrupt transaction

Problem: The processor logs an incorrect request type and address information for a double-bit ECC error on an interrupt or an inbound ptc transaction.

Implication: For a double-bit ECC error on an inbound ptc transaction, the PAL machine check handler may incorrectly raise machine check abort. For a double-bit ECC error on an interrupt transaction, the

processor may incorrectly raise a Corrected Machine Check Interrupt (CMCI) instead of an MCA, leading to possible incorrect functionality.

Workaround: The workaround implemented in PAL release 6.6.23 and 6.6.25 promotes all PAL continuable double-bit ECC system bus errors to OS-recoverable machine check aborts. The MCA logging for double-bit ECC system bus errors may be inaccurate, but errors will be contained. Note: The workaround for this erratum is not included in PAL 6.6.24.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

10. Processor hang during nested BINIT

Problem: On an external assertion of a BINIT non-recoverable MCA within a certain time interval while the processor is servicing a previous external or internally generated BINIT non-recoverable MCA, the system bus may stall due to an infinite assertion of the Block Next Request (BNR)# signal.

Implication: The processor may hang as a result of the nested BINIT condition.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

11. False BIL transactions during PAL_CACHE_FLUSH

Problem: During PAL_FLUSH_CACHE, the processor may issue BIL transactions to incorrect addresses when run in cacheable mode with inv = 1. Although the false BIL transaction is issued, actual data is not modified and cache coherency is still maintained.

Implication: False BIL transactions may be seen on the system bus during execution of the PAL_CACHE_FLUSH call.

Workaround: Since the false BIL always targets a certain address range, depending on how PAL is mapped to writeback memory, the chipset can ignore any bus transactions issued by the processor to that address range.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

12. ALL_STOPS_DISPERSED and EXPL_STOPS_DISPERSED not operating correctly

Problem: The performance monitoring event ALL_STOPS_DISPERSED counts the implicit and explicit stops dispersed, while the event EXPL_STOPS_DISPERSED counts the explicit stops dispersed. These counters incorrectly count their respective events.

Implication: These performance monitoring events may report an incorrect count.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

13. Snoop hit to modified line in L2 cache with tag parity error

Problem: On a snoop hit to a modified line in the L2 cache which encounters a tag parity error, the processor may incorrectly report the snoop response as a miss and hang. The processor does flag an MCA and raise Bus Error (BERR) as expected.

Implication: The processor may hang as a result of encountering a snoop hit to a modified line in the L2 cache with a tag parity error. Also, since the L2 cache reports the snoop response as a miss, another processor can potentially modify the data for that cache line.

Workaround: Enable BERR to BINIT promotion using the PAL_PROC_SET_FEATURES call.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

14. Infinite DBSY# hang due to livelock condition

Problem: In the event of several internal conditions and the specific alignment of these conditions, the processor may encounter a potential livelock. The conditions involve a stream of L3 cache traffic, victimization of modified lines from the L3 cache, a pending L2 cache fill, and a snoop request from an external bus agent that hits the same pending L2 cache line.

Implication: As a result of the livelock condition, the processor asserts the Data Bus Busy (DBSY#) signal without a corresponding data transfer, causing the system to hang. This erratum has only been observed running a synthetic cache stress test.

Workaround: The workaround for this erratum may be enabled with PAL 6.6.21 and later versions. Note: Intel recommends disabling this workaround.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

15. Unexpected writeback transaction in 2:11 mode with bus parking enabled

Problem: Following are the necessary conditions for this erratum:

- The processor is configured in 2:11 bus-to-core ratio and bus parking is enabled.
- One processor Px owns two cache lines A and B in the M-state.
- A snoop request (due to BIL/BRIL transaction) for cache line A followed by a snoop request (due to BIL/BRIL transaction) for cache line B is made (by priority agent or processor Py).
- A specific timing relationship of IDS#, ADS#, and BPRI#/BRy# signals needs to be met.
- In parallel, Px tries to issue an explicit writeback for A followed by an explicit writeback for B.

As a result, the processor may incorrectly issue an explicit writeback transaction for B on the system bus, following the implicit writeback for A and B, which is a violation of the system bus protocol. In addition, the explicit writeback transaction for B may contain incorrect data.

If the processor has another read/write request that needs to be issued to the system bus immediately after the explicit writeback transaction for B, the request may be held pending indefinitely in the processor bus queue causing the processor to hang.

Implication: The processor may issue an explicit writeback transaction with incorrect data when it is not expected to do so. In the case where the read/write request is held pending indefinitely inside the processor, the system may hang. This erratum has only been observed running a synthetic stress test.

Workaround: The workaround for this erratum is to disable bus parking.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

16. IA-32: Code with FP instruction followed by integer instruction with interrupt pending may not execute correctly

Problem: In the event of certain internal conditions, IA-32 code that contains a floating-point instruction followed immediately by an integer instruction with an interrupt pending may not execute correctly.

Implication: IA-32 floating-point code in the above scenario may not execute correctly.

Workaround: A workaround for this erratum is implemented in PAL release 6.6.23.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

17. Bus parking always enabled and not controllable by PAL

Problem: The processor can be configured to not park on the request bus when idle, if A15# is sampled deasserted at the asserted-to-deasserted transition of RESET#. Due to this erratum, PAL overrides the hardware setting and enables bus parking by default. Additionally, the PAL_BUS_GET_FEATURES call reports that bus parking (bit 29) is not controllable and does not allow the PAL_BUS_SET_FEATURES call to enable or disable bus parking.

Implication: PAL enables bus parking by default and overrides the hardware setting at reset. Additionally, bus parking cannot be controlled using the PAL_BUS_SET_FEATURES call.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

18. IA-32: FSINCOS may not generate FP precision exception

Problem: The IA-32 FP instruction, FSINCOS computes both the sine and cosine of a source operand, with the final floating-point operations in the computation expected to generate a precision exception. For certain source operand values, these final operations may be computed exactly, causing the expected floating-point precision exception not to be generated.

Implication: For certain source operands, the FSINCOS instruction fails to generate the expected floating-point precision exception.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

19. chk.a.clr/ld.c.clr incorrectly clears its ALAT entry

Problem: Under certain conditions following the execution of an advanced load, the speculation check instructions, chk.a.clr and ld.c.clr, may incorrectly report a miss in the Advanced Load Address Table (ALAT) indicating that the data speculation was unsuccessful.

Implication: As a result of the miss, the check load (ld.c) will reload the correct value from memory and the advanced load check (chk.a) will branch to compiler-generated recovery code.

Workaround: Replace chk.a.clr with chk.a.nc, and ld.c.clr with ld.c.nc.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

20. IA-32: Back to back semaphores under certain circumstances may cause processor to hang

Problem: In the event of certain internal conditions involving the processor Virtual Hash Page Table (VHPT) walker, while the processor is executing a sequence of back-to-back IA-32 semaphore operations, the processor may hang.

Implication: IA-32 code operating on locked semaphores in the above scenario may cause the processor to hang. Note: Typical spin lock code containing semaphores is not affected by this erratum. This erratum has only been observed running a focused test in a system validation environment.

Workaround: Separate back-to-back IA-32 semaphores with a minimum of two NOPs.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

21. Modification of PFS under certain circumstances can lead to unexpected program behavior

Problem: The Previous Function State register (PFS) is provided to accelerate procedure calling. Under certain circumstances involving a specific code sequence, and a set of internal architectural and timing conditions, modification of the PFS fields prior to br.ret may result in incorrect restoration of state on returning back to the caller procedure.

Implication: Execution of code that meets the above criteria may result in unexpected program behavior. The erratum is not exposed for typical code involving PFS restoration identical to the initial PFS value stored on a procedure call, or code that creates a new stack frame by loading a new CFM to PFS prior to br.ret. This erratum has only been observed running a focused test in a system validation environment.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

22. Corrected machine check not indicated when CMCI is promoted to MCA

Problem: When correctable machine check interrupts (CMCIs) are promoted to machine check aborts (MCAs) through the PAL_PROC_SET_FEATURES call, on a corrected machine check error it is possible for PAL to not set the “cm” bit of the processor state parameter (PSP) at PALE_CHECK exit to indicate that the machine check has been corrected.

Implication: The indication that a machine check error has been corrected may not be provided in this case.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

23. PAL_MC_ERROR_INFO may return incorrect target address information

Problem: The PAL_MC_ERROR_INFO call returns the error information on a processor machine check. When a system bus or an L3 cache machine checks occur, the PAL_MC_ERROR_INFO call may not report the target address correctly.

Implication: The target address information for system bus or L3 cache machine checks may be incorrectly logged.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

24. Incorrect store update to L1D cache under certain circumstances

Problem: In the case of back-to-back stores that hit the L1 data cache (L1D), it is possible under certain circumstances for the data corresponding to one of the stores to be overwritten by a later store before it is updated in the cache. The necessary conditions for this erratum involve a stream of stores that hit the L1D cache with address dependencies amongst them and require specific internal timing conditions to be met.

Implication: A store may be incorrectly overwritten before it is updated in the cache. This erratum has only been observed running a synthetic test in a system validation environment.

Workaround: The workaround can be enabled by SAL using PAL 6.6.21 and PAL 6.6.23 and is enabled by default in PAL 6.6.24 and later versions.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

25. IA-32: Unexpected page fault exception on SETcc instruction

Problem: Under specific conditions, if an IA-32 SETcc instruction is operating on self-modifying code (SMC) and the memory being stored by the SETcc instruction encounters a segment limit violation, the limit violation exception may not be taken and instead a page fault exception is taken.

Implication: IA-32 applications that execute SMC and encounter a segment limit violation would result in a GP fault, which is a non-recoverable condition for the application. The page fault exception will result in the same behavior. This erratum has only been observed during random instruction testing in a system validation environment.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

26. IA-32: PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ reads 8 bytes instead of 4 bytes

Problem: If the source data for the IA-32 MMX(TM) Technology instructions, PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ comes from memory, the processor should access only 32-bits from memory. Due to this erratum, the processor always accesses 64-bit data from memory, even though only 32-bits are used (no operation is performed on the 4 extra bytes).

Implication: If the memory address being accessed is close to the segment limit, a limit violation exception may be generated. In the case where the 4-byte data being accessed is located at the end of a page and the next page is invalid, an unexpected page fault may be generated. This erratum has only been observed during random instruction testing in a system validation environment.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

27. Processor may incorrectly report an IA-32 BIST failure

Problem: If Built-in Self Test (BIST) is enabled through INIT# pin signalling at reset, the processor may incorrectly report an IA-32 BIST failure.

Implication: Even though BIST executes correctly, the processor may incorrectly report an IA-32 BIST failure.

Workaround: If BIST is enabled, the firmware (SAL), upon reading the BIST result, can ignore any IA-32 BIST failure.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

28. Back-to-back pair of loads to L1D cache result in possible livelock condition

Problem: In the event of certain internal conditions, the processor may encounter a livelock during lookup in the L1 data cache. The livelock condition may occur if the processor is executing a code sequence which contains a back-to-back pair of load instructions with all the load addresses hitting the L1 data cache and there is a specific relationship between the virtual addresses for these loads.

Implication: Because the processor continues to take interrupts during the livelock, the livelock condition will likely be broken when an interrupt is received or when there is a context switch to another process. In the case where the livelock condition is not broken, the processor may hang and eventually time-out (if internal processor time-out is enabled) generating a BINIT. This erratum has only been observed running a synthetic test in a system validation environment.

Workaround: A workaround for this erratum will be implemented in a future PAL release.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

29. PAL_PERF_MON_INFO returns incorrect information on registers which can count retired instruction bundles

Problem: The PAL_PERF_MON_INFO procedure is called to determine the number of performance monitors and the events which can be counted on the performance monitors. Due to this erratum, the PAL_PERF_MON_INFO procedure returns PMC4 as the only register available to count retired instruction bundles instead of returning PMC4 and PMC5.

Implication: The information returned by the PAL_PERF_MON_INFO call on the number of registers available for counting retired instruction bundles is incorrect.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

30. ALAT not guaranteed to be invalidated by an external snoop under specific conditions

Problem: Under certain conditions involving the timing of an advanced load instruction (`ld.a`) overlapping with an external snoop caused by a store (from another processor) to the same address as that of the advanced load, the Advanced Load Address Table (ALAT) may not get invalidated correctly by the external snoop.

Implication: As a result of this erratum, when operating in an MP environment, any advanced load boosted ahead of any acquire (including fences, mfa etc.) does not guarantee coherent ordering as shown in the code sequence below. This includes any advanced loads boosted ahead of any function call where the function may include memory ordering ops with acquire semantics:

```
Processor 0                                   Processor 1
ld.a X                                        st X
<any ordered op with acquire semantics>
ld.c X

Note: In the above example, the external snoop to processor 0 is a result of
store to address X by processor 1.
```

The affected code sequence is not known by Intel to be generated in any current OS or compiler.

Workaround: To avoid this erratum, compilers and hand-written code should not boost an advanced load ahead of any ordered op with acquire semantics or ahead of opaque function calls.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

31. WC store may be dropped under certain conditions

Problem: Under certain conditions involving Write Coalescing (WC) stores, a check load (`ld.c`) or an `lfetch` instruction interspersed with stores to WC space, may result in one of the WC stores to be dropped. This may occur in the following scenario:

- A store to WC space (A) is followed one or more instructions later by a `ld.c` or an `lfetch` to WC space which is to an address in the same WC buffer entries as store A.
- This `ld.c` (or `lfetch`) to WC space is followed by another WC store (B) either in the same instruction group, or in one instruction group later. Store B is to an address also in the same WC buffer entries as store A.

Implication: Code operating in WC space in the above scenario may not execute correctly. Note: Typical usage of WC memory is by device driver code for graphics adaptors or graphics texture mapping code and consists mostly of store operations. This erratum has only been observed running a focused test in a system validation environment.

Workaround: None identified at this time.

Status: For the steppings affected, see the Summary Table of Changes at the beginning of this section.

Specification Changes

There are no Specification Changes for this revision of the *Intel® Itanium™ Processor Specification Update*.

Specification Clarifications

There are no Specification Clarifications for this revision of the *Intel® Itanium™ Processor Specification Update*.

Documentation Changes

There are no Documentation Changes for this revision of the *Intel® Itanium™ Processor Specification Update*.